In re Patent Application of
GENDRIER ET AL.
Serial No. 10/511,712
Filed: OCTOBER 15, 2004

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application, for correctly withdrawing the previous rejections of the claims, and for indicating that dependent Claims 35-67 and 69-100 recite patentable subject matter.

Applicants have amended independent Claims 34 and 68 to more clearly define the claimed invention over the prior art. Applicants submit that all claims are patentable and present arguments and amendments herein supporting such patentability.

I. The Claimed Invention

Amended independent Claim 34 is directed to a semiconductor memory device comprising an electrically erasable and programmable non-volatile memory cell. The memory cell includes a layer of gate material and a floating-gate transistor including a floating gate defined in the layer of gate material, a source, a drain, and channel regions defining a control gate. The memory cell further includes a first active zone, a second active zone incorporating the control gate and electrically isolated from the first active zone, and a dielectric zone between a first part of the layer of gate material and the first active zone. The dielectric zone defines a transfer zone for transferring, during erasure of the memory cell, charges stored in the floating gate to the first active zone. Amended independent Claim 68 is a method counterpart to Claim 34.

During erasure of the memory cell, the charges are no longer extracted through a gate oxide of the floating-gate transistor but through a dielectric zone, which is located opposite an active zone electrically isolated from the active zone incorporating the control gate, and consequently the source, channel and drain regions of the floating-gate transistor. Hence, according to the claimed invention, degradation of the oxide in the tunnel zone does not cause the transistor of the cell to undergo aging.

II. The Claims Are Patentable

The Examiner rejected independent Claims 34 and 68 over Guterman et al. Referring to Figure 1B of Guterman et al., a memory cell is disclosed and comprises a source 102 and drain 103 with a channel region 106 therebetween, and a dielectric layer over the drain, the source, and the channel. The memory cell further comprises a floating gate 107 formed on the dielectric layer and above the drain, and a control gate 108 formed on the floating gate. (Guterman et al.: Col. 5, line 48 through Col. 6, line 13). During operation, charges are tunneled from the source side of the channel 106-2 through the dielectric layer to the floating gate. (Col. 6, lines 15-29).

In contrast, amended independent Claims 34 and 68 recite the source, the drain, and channel regions defining a control gate. In the claimed device, because the control gate is defined by the source, drain, and channel regions of the floating-gate transistor, the memory cell is erased by applying a voltage to the first active zone that is much

higher than the voltages applied to the source, drain, and channel regions of the transistor. (Present Application: Paragraph 52). The control gate of Guterman et al. is not defined by the source, the drain, and the channel regions. (Figures 1A & 1B). Indeed, Guterman et al. discloses applying a lower voltage to the distinct control gate adjacent the floating gate for forcing charge from the source side of the channel through the dielectric layer and into the floating gate. Therefore, for this reason alone, independent Claims 34 and 68 are patentable.

Moreover, Guterman et al. does not disclose the second active zone incorporating the control gate and electrically isolated from the first active zone, as in the claimed invention. Differently, Guterman et al. discloses tunneling charges from the source side of the channel through the dielectric layer to the floating gate. (Guterman et al.: Col. 6, lines 15-29). In an attempt to provide the first and second active control regions of the claimed invention, the Examiner looked to a different embodiment of Guterman et al. depicted in Figures 9a-b and cited the POLY3 region as providing the first active zone. This embodiment also discloses source side tunneling during operation for programming and poly-to-poly tunneling for erasure. (Col. 17, lines 63-68).

The POLY3 region (cited by the Examiner as disclosing the first active zone) provides the control gate of the memory cell, i.e. erasure node being brought to a certain potential to erase the memory cell. (Col. 19, lines 25-34). In other words, Guterman et al. does not disclose the second

active zone incorporating the control gate, as in the claimed invention. The Examiner cited no region in either embodiment of Guterman et al. for the second active zone. Accordingly, for this additional reason, Guterman et al. does not disclose the claimed invention, and amended independent Claims 34 and 68 are patentable.

Accordingly, it is submitted that amended independent Claims 34 and 68 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

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CONCLUSIONS

In view of the arguments and amendments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 29th day of August, 2007.